Course Logistics:

Credit Hours: 3

Lectures:
- MON 1:00 PM - 1:50 PM (NSC 228)
- WED 1:00 PM - 1:50 PM (NSC 228)
- FRI 1:00 PM - 1:50 PM (NSC 228)

Instructor (332 Davis Hall):
Farshad Ghanei (farshadg@buffalo.edu)  MON, TUE  2:00 PM – 3:30 PM

Teaching Assistants:
- Yang Gao (ygao36@buffalo.edu)  THU 3:00 PM – 5:00 PM (Davis 3xx)
- Yuyang Chen(yuyangch@buffalo.edu)  WED 2:00 PM – 4:00 PM (Davis 3xx)
- Ian Kaminer (iankamin@buffalo.edu)  MON 3:30 PM – 5:00 PM (Bonner 114)

Exam Schedule:
- Midterm Exam-1:  WED March 11th  NSC 228 @ 1:00 PM - 1:50 PM
- Midterm Exam-2:  WED April  22nd  NSC 228 @ 1:00 PM - 1:50 PM
- Final Exam:  FRI May  15th  NSC 228 @ 11:45 AM - 2:45 PM

Note: If you need to email course staff, please include [CSE 490] or [CSE 590] at the beginning of the subject line so your email is not missed. Emails without this subject or from non-UB accounts will be ignored.

Course Description:

This is an advanced course in computer architecture. Students will learn how modern processors and systems are designed. They will gain both theoretical and hands-on experience. Topics covered include: pipelining, memory and I/O subsystems (including content addressable memories), superscalar organization and design techniques, advanced instruction flow and register data flow techniques, multiple thread execution, hardware description languages, CPLDs and FPGAs.

Course Prerequisites:

CSE 379 Introduction to Microprocessors, CSE 341 Computer Organization, or an equivalent course, or permission of the instructor.
Learning Outcomes:
At the end of this course, a successful student should be able to:

- Understand how a modern processor and system is designed.
- Explain how superscalar processors are organized and designed.
- Design a memory subsystem for a computer.
- Understand advanced instruction flow and register data flow techniques.
- Design a circuit and simulate it using an HDL.
- Design a system to implement a specific task and implement the design on an FPGA or CPLD.
- Incorporate all of the above into designing a system.

Textbook:
Modern Processor Design – Fundamentals of Superscalar Processors
ISBN: 978-1-4786-0783-0

Additional Required Materials:
- Basys 3 Atrix-7 FPGA Trainer Board from Digilent, Inc.
- Xilinx Vivado WebPack

References:
- Volnei A. Pedroni, Circuit Design with VHDL, MIT Press 2004
- Enoch O. Hwang, Digital Logic and Microprocessor Design with VHDL, Thomson Canada Limited, 2006
UB Portfolio:
If you are completing this course as part of your UB Curriculum requirements, please select an ‘artifact’ from this course that is representative of your learning and upload it to your UBPortfolio (powered by Digication) account. Templates have been created for this purpose. Artifacts include homework assignments, exams, research papers, projects, lab reports, presentations, and other course materials. Your final UB Curriculum requirement, UBC 399: UB Curriculum Capstone, will require you to submit these ‘artifacts’ as you process and reflect on your achievement and growth through the UB Curriculum. For more information, see the UB Curriculum Capstone website: https://www.buffalo.edu/ubcurriculum/capstone.html

Piazza Discussion Forum:
We will use Piazza for class discussion. The system is highly efficient and faster, in order to ask your questions from classmates or teaching staff. https://piazza.com/buffalo/spring2020/cse490590

Accessibility Resources:
If you have any disability which requires reasonable accommodations to enable you to participate in this course, please contact the Office of Accessibility Resources in 60 Capen Hall, 716-645-2608 and also the instructor of this course during the first week of class. The office will provide you with information and review appropriate arrangements for reasonable accommodations, which can be found on the web at: http://www.buffalo.edu/studentlife/who-we-are/departments/accessibility.html

Course Requirements:
The following items are required of every student, and failure to complete them may affect student grades:

General: Attendance in this course is mandatory, but will not necessarily be directly tracked. Students are responsible for attending every lecture. It will be assumed that students are familiar with all material presented in class, and any material presented in lecture may appear on any test, quiz, homework assignment, or other evaluation. Attendance and attention to lecture are critical to success in this course.

Exams and Pop Quizzes: There will be 7 pop quizzes taken throughout the semester. Two with the lowest grades will be discarded and the rest five will count towards your final grade. The questions are mostly from material discussed in the previous lectures
or homework assignments. The quizzes are very short (5-10 minutes) with one or two questions aiming to test whether you have understood the discussed concepts. There will be two mid-term exams taken during two of the lectures. All tests are to be taken individually and without the use of any resource such as books/computer/internet. Exams and quizzes may be video-recorded. These videos are not meant to be uploaded anywhere. But they are to ensure the integrity of the test.

**Homework:** There will be 5 homework assignments throughout the semester. The homework assignments are not graded, they aim to ensure that you study regularly for the material covered in class.

**Projects:** There will be two projects throughout the course. One is to familiarize you with the trainer board and VHDL, and one is more substantial and constitutes an important part of your overall grade.

**Late Submission Policy:**
* There will be no late submissions allowed.

**Exam Policy:**
* No makeup exams will be given except in provably extreme circumstances.
* Notify your instructor 24 hours prior to the exam via e-mail if you are going to miss an exam. If it is medically impossible for you to give prior notice, please obtain a note from a physician detailing the period (and the reason) you were medically incapable of communicating with the instructor.
* If you miss an examination because of sickness or similar reasons, visit a physician and obtain a note detailing the period and the reason you were medically incapable of taking the exam.
* You are responsible for knowing about the exam dates: you will get plenty of notice about the exam dates. Please plan your travel and other activities accordingly.
* Exam times are stressful and one could forget about the exam time. Please make sure you arrange for multiple reminders so that you do not forget about the exams.
Grading Policy:

Each student’s grade is computed from a weighted average of the following items:

- Project-1: 10%
- Project-2: 30%
- Midterm Exam-1: 20%
- Midterm Exam-2: 20%
- Final Exam: 20%
- Pop Quizzes: 5% Extra (5 out of 7 Quizzes)
- Homework: 0% (5 Homework assignments, not graded)

The final letter grade is based upon the following cutoffs:

- 93+ A
- 90-92 A-
- 87-89 B+
- 83-86 B
- 80-82 B-
- 77-79 C+
- 73-76 C
- 70-72 C-
- 67-69 D+
- 60-66 D
- 0-59 F

*If you score less than 20% in either of the projects, you will fail the course independent of overall grade.

* If necessary, the instructor may revise these cutoffs downward.

* There will be separate curves for graduate and undergraduate students at the end of the semester to address inconsistencies or hardships that arise. Grades will not be curved/adjusted during the semester.

* Attending the class and active participation is highly recommended and expected.
* If there is any issue with grading, contact the teaching staff within 2 weeks of posting them.

* Students will receive a grade of “F” if they are found in violation of the academic integrity policy. Please make sure to thoroughly read and understand the policy for this course.

Incompletes (I/IIU): The course follows the university undergraduate incomplete policy. A grade of incomplete (“I”) indicates that additional coursework is required to fulfill the requirements of a given course. Students may only be given an “I” grade if they have a
passing average in coursework that has been completed and have well-defined parameters to complete the course requirements that could result in a grade better than the default grade. An “I” grade may not be assigned to a student who did not attend the course. Prior to the end of the semester, students must initiate the request for an “I” grade and receive the instructor’s approval. Assignment of an “I” grade is at the discretion of the instructor. Upon assigning an “I” grade, the instructor shall provide the student specification, in writing or by electronic mail, of the requirements to be fulfilled, and shall file a copy with the appropriate departmental office. Students must not re-register for courses for which they have received an “I” grade.

**Failure for Non-Attendance (FX):** Students who have earned a failing grade due to lack of attendance (or participation where attendance is no applicable) will be awarded an “FX”.

**Academic Integrity Policy:**

Academic integrity is a fundamental university value. Through the honest completion of academic work, students sustain the integrity of the university while facilitating the university’s imperative for the transmission of knowledge and culture based upon the generation of new and innovative ideas. Students will abide by the CSE Academic Integrity Policy, the University Academic Integrity Policy, and the Undergraduate or Graduate amendments thereof, as appropriate. All resources used in completing assignments for this class must be given appropriate attribution, and the only resources allowed for the completion of programming assignments without specific permission are as follows.

- The course textbook
- Lecture material from this course
- Resources provided by the teaching staff for assignments.

In particular, Stack Exchange, code from other students in the course or students who have completed this course or related courses at other universities in previous semesters, GitHub repositories, code or algorithms from other websites or books, and other resources are not allowed without explicit permission from the instructor. If there is any question about whether a resource is acceptable for use in completing a course assignment, students are encouraged to ask the instructor or a TA before making use of it. Asking about a resource is not a violation of academic integrity, even if the resource is not allowed for the course.

Violation of these policies will result in a failing grade for the course and referral upward for additional sanctions according to University policy.

As an engineer or computer scientist, you have special ethical obligations. As per the NSPE Code of Ethics, “engineers shall avoid deceptive acts” and “shall conduct themselves honorably, responsibly, ethically, and lawfully so as to enhance the honor,

Note: We use professional software which can easily detect any cheating attempts in programming projects. The results generated by this software is considered as official evidence for cheating from another student, or from internet sources.

Academic Integrity Amnesty:
A student who has committed a violation of this academic integrity policy may receive limited amnesty for the violation by notifying me, in writing, of the violation before I have begun to assess the violating assignment. This notification must include the student’s name, person number, UBITname, and state the assignment in question and the nature of the violation. Upon submitting such a statement, the student will receive no credit for the violating assignment, but no further sanctions will be taken, and the violation will not be reported. Once I have begun assessing the assignment in question, no such statements will be permitted. Since it may not be obvious to students when assessment begins, such statements should be submitted as soon as possible after the violation occurs. While assessment may begin at any time, in general I will not look at student submissions until a project deadline has passed.

Classroom Decorum:
Meaningful and constructive dialogue is encouraged in this class and requires a degree of mutual respect, willingness to listen, and tolerance of opposing points of view. Respect for individual differences and alternative viewpoints will be maintained at all times in this class. One's words and use of language should be temperate and within acceptable bounds of civility and decency. Since every student is entitled to full participation in class without interruption, all students are expected to come to class prepared and on time, and remain for the full class period. All pagers, wireless phones, games, players or other electronic devices that generate sound and/or pictures must be turned off during class. Disruptive behaviors, including excessive talking, arriving late to class, sleeping, reading newspapers, using unauthorized electronic devices during class is not permitted. Repetitive and seriously disruptive behavior, e.g., fighting, using profanity, personal or physical threats or insults, damaging property, may result in your removal from class in accordance with policies and procedures outlined in university policies. Further consequences may be applied through Student Conduct Regulations handled by the Office of Student Conduct and Advocacy. Substantial issues will be handled through the University Police Department.
Copyright Policy:

Materials used in connection with this course may be subject to copyright protection under Title 17 of the United States Code. Under certain Fair Use circumstances specified by law, copies may be made for private study, scholarship, or research. Electronic copies should not be shared with unauthorized users. If a user fails to comply with Fair Use restrictions, he/she may be liable for copyright infringement.

Critical Campus Resources:

Sexual Violence: UB is committed to providing a safe learning environment free of all forms of discrimination and sexual harassment, including sexual assault, domestic and dating violence and stalking. If you have experienced gender-based violence (intimate partner violence, attempted or completed sexual assault, harassment, coercion, stalking, etc.), UB has resources to help. This includes academic accommodations, health and counseling services, housing accommodations, helping with legal protective orders, and assistance with reporting the incident to police or other UB officials if you so choose. Please contact UB’s Title IX Coordinator at 716-645-2266 for more information. For confidential assistance, you may also contact a Crisis Services Campus Advocate at 716-796-4399.

Mental Health: As a student you may experience a range of issues that can cause barriers to learning or reduce your ability to participate in daily activities. These might include strained relationships, anxiety, high levels of stress, alcohol/drug problems, feeling down, health concerns, or unwanted sexual experiences. Counseling, Health Services, and Health Promotion are here to help with these or other issues you may experience. You can learn more about these programs and services by contacting:

Counseling Services:
* 120 Richmond Quad (North Campus), 716-645-2720
* 202 Michael Hall (South Campus), 716-829-5800

Health Services:
* Michael Hall (South Campus), 716-829-3316

Health Promotion:
* 114 Student Union (North Campus), 716-645-2837

Acknowledgments:

Majority of the materials offered in this course is obtained from Dr Schindler. I truly appreciate their support and guidance, which has helped me offer this course more effectively.

Some language in this syllabus is drawn from University policies (as noted), the UB Course Syllabi Requirements document, department guidelines, and other University resources. Some language and structure in this syllabus is drawn from syllabi of CSE faculty members: Dr Schindler, Dr Ko, Dr Dantu, Dr Blanton, Dr Winikus, Dr Hertz.
*All content in the syllabus is subject to change based on the needs of the class and the discretion of the instructor*

**Course Schedule**
This schedule is subject to change. Please check Piazza for announcements and course material.

<table>
<thead>
<tr>
<th>Date/Day</th>
<th>Lecture</th>
<th>Title</th>
<th>Notes</th>
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<tbody>
<tr>
<td>Jan 27</td>
<td>M</td>
<td>1 Introduction</td>
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<tr>
<td>Jan 29</td>
<td>W</td>
<td>2 Review of Binary Arithmetics, etc.</td>
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<td>Jan 31</td>
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<td>3 Review of Flip-Flops, etc.</td>
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<td>Feb 3</td>
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<td>4 Review of Logic Circuits</td>
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<td>Feb 5</td>
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<td>5 Datapath Discussion</td>
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<td>6 CAD Tools</td>
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<td>Feb 10</td>
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<td>Feb 12</td>
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<td>8 Structural VHDL</td>
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<td>Feb 14</td>
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<td>Feb 21</td>
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<td>12 Basys 3 Board</td>
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<td>Feb 24</td>
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<td>Feb 26</td>
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<td>Feb 28</td>
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<td>Mar 2</td>
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<td>Mar 4</td>
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<td>Mar 6</td>
<td>F</td>
<td>18 Memory &amp; I/O-2</td>
<td>Project-1 due</td>
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<td>Mar 9</td>
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<td>19 Midterm Exam-1 Review</td>
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<td>Mar 11</td>
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<td>Midterm Exam-1 (NSC 228 @ 12:30)</td>
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<td>Mar 13</td>
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<td>20 Project-2 Discussion</td>
<td>Project-2 out</td>
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<td>Spring Recess</td>
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<td>21 Memory &amp; I/O-3</td>
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<td>Mar 27</td>
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<td>Mar 30</td>
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<td>Apr 1</td>
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<td>25 Superscalar Architectures-2</td>
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<td>Apr 3</td>
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<td>26 Superscalar Architectures-3</td>
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<td>27 Superscalar Architectures-4</td>
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<td>Apr 10</td>
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<td>Apr 17</td>
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<td>32 The FPGA Overview</td>
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<td>Apr 20</td>
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<td>33 Midterm Exam-2 Review</td>
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<td>Apr 22</td>
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<td>34 The FPGA-1</td>
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<td>May 4</td>
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<td>May 6</td>
<td>W</td>
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<td>May 8</td>
<td>F</td>
<td>40 Performance Discussion</td>
<td>Project-2 due</td>
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<td>May 15</td>
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<td>Final Exam (NSC 228 @ 11:45)</td>
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